FIG. 1

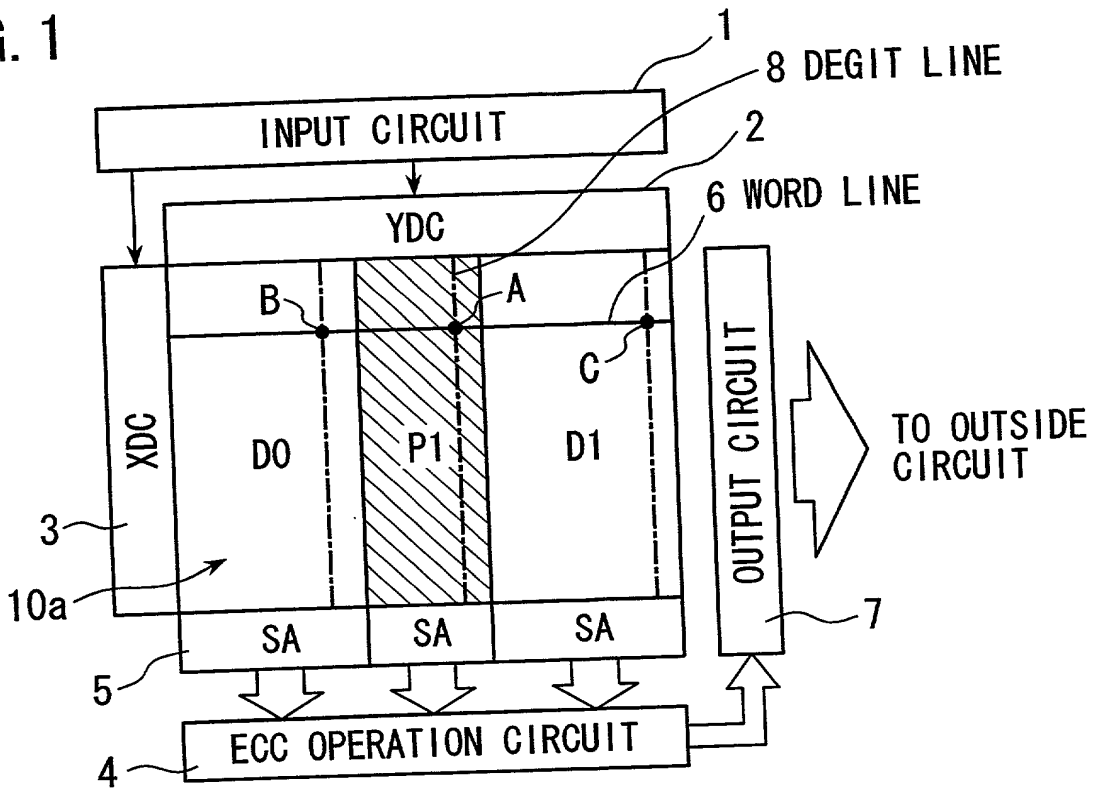

1
8 DEGIT LINE
INPUT CIRCUIT
2
YDC
6 WORD LINE
B
A
C
XDC
DO
P1
D1
OUTPUT CIRCUIT
TO OUTSIDE CIRCUIT
3
10a
SA
SA
SA
7
5
ECC OPERATION CIRCUIT
4

FIG. 2

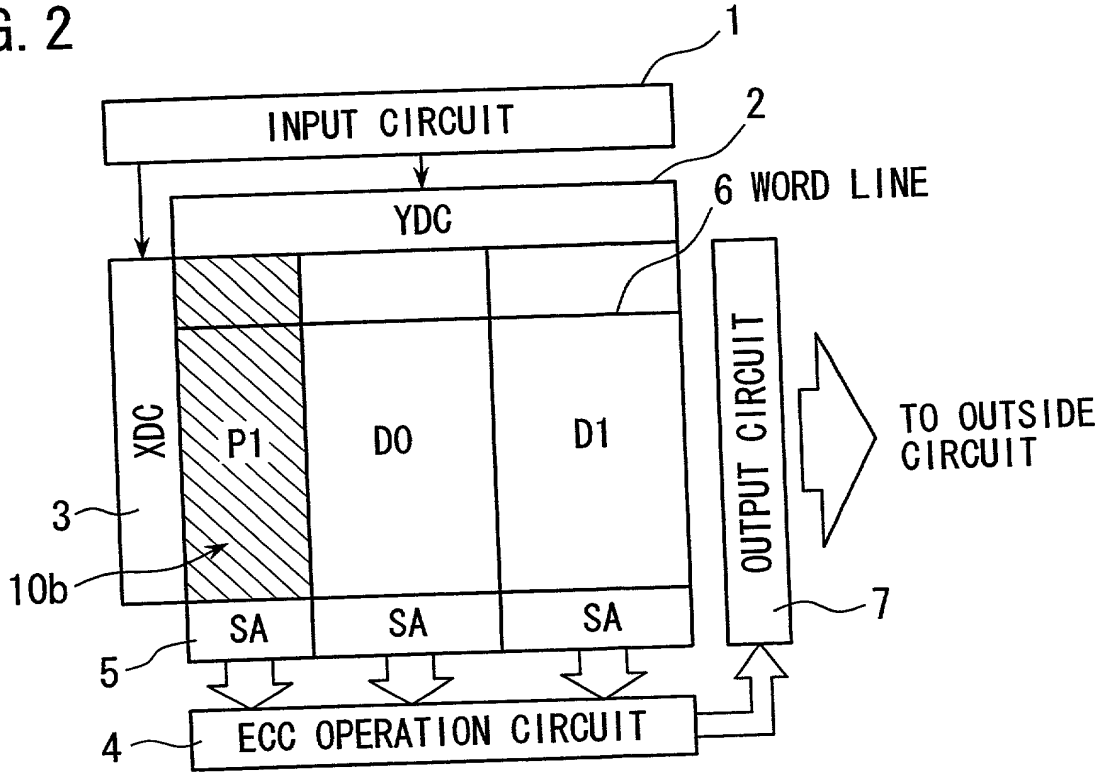
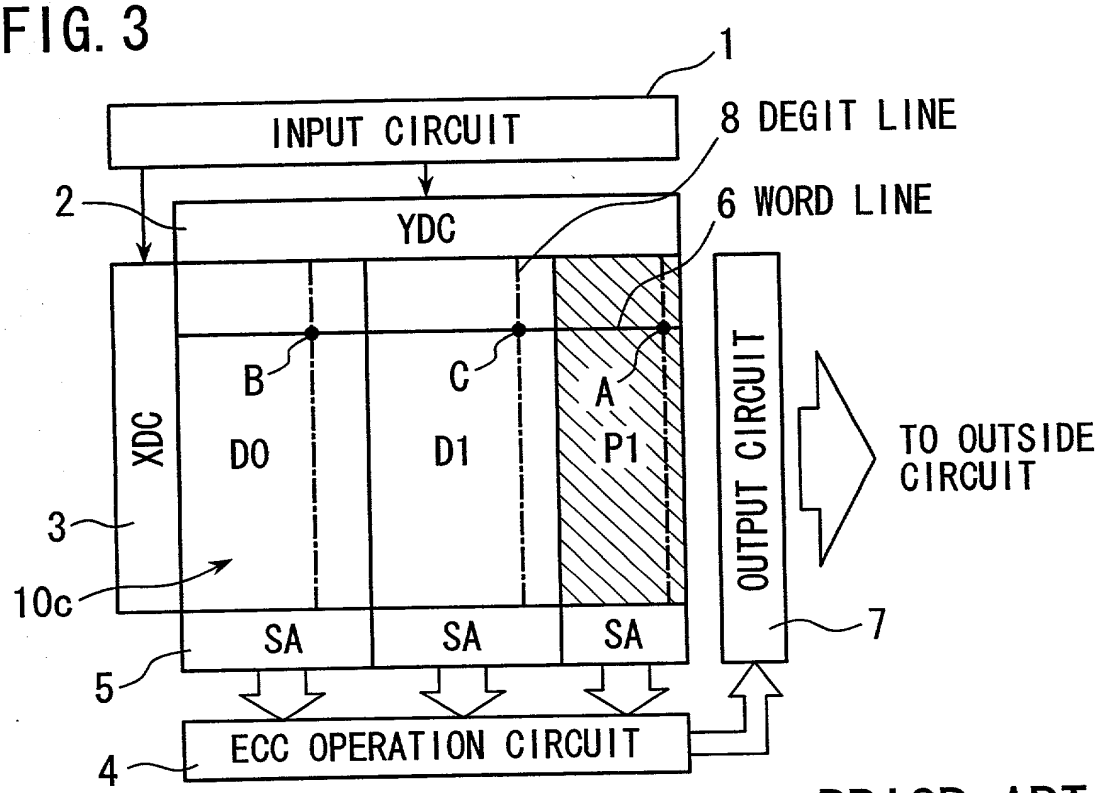
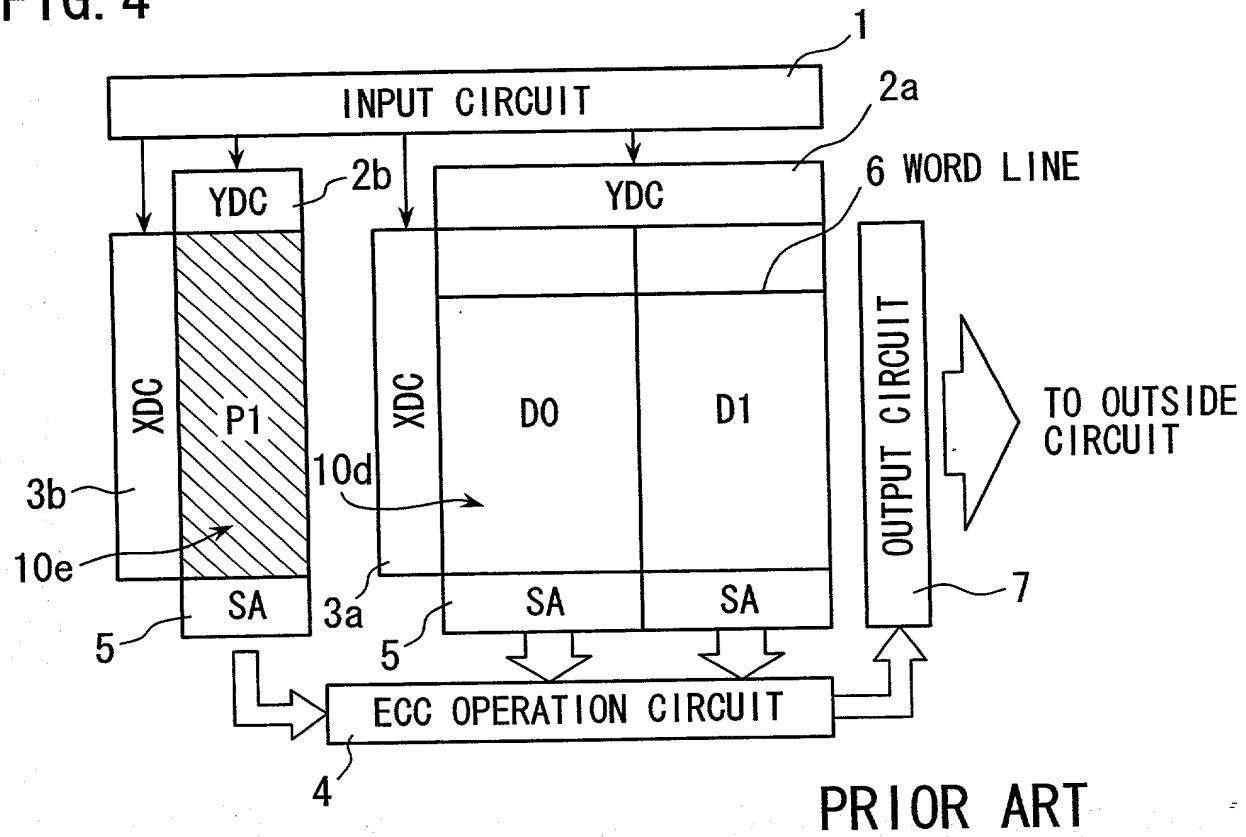

1
INPUT CIRCUIT
2
YDC
6 WORD LINE
XDC
P1
DO
D1
OUTPUT CIRCUIT
TO OUTSIDE CIRCUIT
3
10b
SA
SA
SA
7
5
ECC OPERATION CIRCUIT
4

FIG. 3



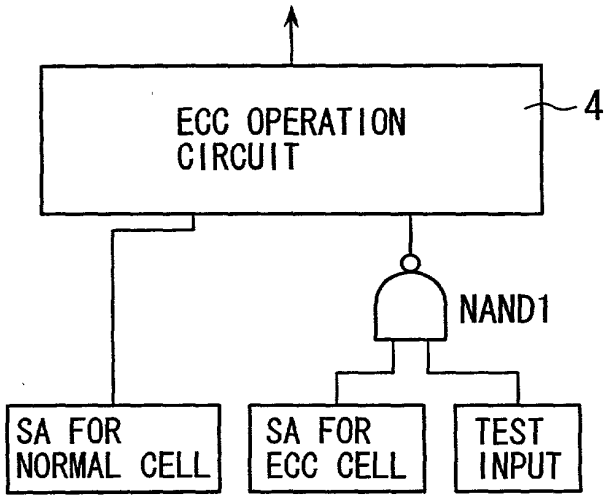
PRIOR ART

FIG. 4



PRIOR ART

FIG. 5



WHEN ECC ENABLED:
TEST INPUT IS VCC → OUTPUT OF NAND1 DEPENDS ON ECC CELL DATA

WHEN ECC DISABLED:
TEST INPUT IS GND → OUTPUT OF NAND1 IS ALWAYS HIGH

PRIOR ART